

REMARKS

Applicant respectfully requests reconsideration and allowance of claims 1-3, 5-17 and 21-25 which are pending in the above-identified application. Applicant has cancelled claims 4 and 19, amended claims 1, 5, 15, 21, 22, and added new claim 25.

In parts 2-5 of the Office Action, the Examiner rejected claims 21-24 under 35 U.S.C. §112, second paragraph, as being indefinite. In particular, the Examiner stated that in claim 21 the phrase "the digital data" in lines 3 and 9 had no antecedent basis. Applicant has amended claim 21, line 6 to recite "the digital data words", which phrase has antecedent basis in the preamble. Applicant has reviewed claim 21, lines 3 and 9 and was unable to locate a recitation of "the digital data." Accordingly, Applicant believes that claim 21 is definite.

The Examiner rejected claim 22 under §112 for omitting essential structural cooperative relationships of elements. In response, Applicant has amended claim 22 to include that the shift register is "operatively coupled to the ALU", which language particularly points out the structural cooperative relationships between the shift register and the apparatus of independent claim 15. Accordingly, Applicant submits that claim 22 is definite.

In parts 6 and 7 of the Office Action, the Examiner rejected claims 1-3, 7-17 and 21 under 35 U.S.C. §103(a) as being unpatentable over the Birman reference in view of the Wong

reference and the Doyle reference. Applicant respectfully traverses the Examiner's rejection.

Each of independent claims 1, 15 and 21 have been amended hereinabove to include that the ALU has "at least three operand inputs" and is "capable of receiving a plurality of bits which define a three port parametrised logic function to be performed on the at least three operand inputs and being capable of executing the three port parametrised logic function." Neither the Birman, Wong nor Doyle references (alone or in combination) disclose or suggest the above quoted limitation. Accordingly, Applicant submits that independent claims 1, 15 and 21 are patentable over the cited combination.

Further, claims 2-3 and 7-14 depend from independent claim 1 and contain all of the limitations thereof as well as other limitations which are neither disclosed nor suggested in the prior art of record. Claims 16 and 17 depend from independent claim 15 and contain all of the limitations thereof as well as other limitations which are neither disclosed nor suggested in the prior art of record. Accordingly, Applicant submits that the subject dependent claims recite patentable combinations.

In part 8 of the Office Action, the Examiner rejected claims 4 and 19 under 35 U.S.C. §103(a) as being unpatentable over the Birman reference in view of the Wong reference. Applicant has cancelled claims 4 and 19 herein which renders the Examiner's rejection moot.

In part 9 of the Office Action, the Examiner rejected claim 5 under 35 U.S.C. §103(a) as being unpatentable over the Doyle reference. Applicant respectfully traverses the Examiner's rejection. Claim 5 has been amended herein to include the limitation that "the ALU having at least three operand inputs and being capable of receiving a plurality of bits which define a three port parametrised logic function to be performed on the at least three operand inputs and being capable of executing the three port parametrised logic function." The Doyle reference fails to teach or suggest the above quoted limitation and, therefore, the Examiner's §103(a) rejection of claim 5 should be withdrawn.

In part 10 of the Office Action, the Examiner rejected claim 6 under 35 U.S.C. §103(a) as being unpatentable over the Suzuki reference in view of the Gergen reference. Applicant respectfully traverses the Examiner's rejection. The Examiner contended that, since the Suzuki reference taught the use of a "most significant bit detector", one of ordinary skill in the art would realize that this detector enables shift registers 14, 15, and 17 to receive data words of variable lengths. The Examiner has taken a quantum leap in making this assertion because there is absolutely no teaching in either the Suzuki or Gergen references which shows one skilled in the art how the shift registers would be capable of receiving data words of variable lengths. Indeed, most significant bit detectors are used to determine the location of a most significant bit, not to enable a shift register to receive data words of variable lengths.

Accordingly, the Examiner's 103(a) rejection of claim 6 should be withdrawn.

In part 11 of the Office Action, the Examiner rejected claims 22-24 under 35 U.S.C. §103(a) as being unpatentable over the Birman reference in view of the Wong and Doyle references as applied to claims 1-3, 7-17 and 21 and further in view of the Suzuki and Gergen references as applied to claim 6. Applicant respectfully traverses the Examiner's rejection. As discussed above, claim 15 is patentable over the cited references. Claims 22-24 are dependent from claim 15 and contain all of the limitations thereof as well as other limitations which are neither disclosed nor suggested in the cited combination.

Accordingly, Applicant submits that claims 22-24 are patentable.

Applicant has added new claim 25 which, for the reasons presented hereinabove, is believed patentable over the art of record.

In light of the Amendments made hereinabove, Applicant believes that the instant claims are in condition for allowance. The Examiner is invited to contact the undersigned to discuss any still outstanding matters. Early and favorable action is

earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on August 11, 1997

Matthew B. Dernier

Name of applicant, assignee or  
Registered Representative



Signature  
August 11, 1997

Date of Signature

Respectfully submitted,



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